Industry Standard Architecture (ISA) Based Data Acquisition Card

LOPE BEN C. PORQUIS
OSCAR Y. CHUY

Abstract

This paper was addressed to the problem of producing an inexpensive local counterpart of a Data Acquisition Card that would serve as an interface between the computer and the hardware prototype for real time hardware in-the-loop simulation. The project was developed following two stages: the experimental stage and prototype stage. The C language was used in testing and evaluating the device. The results of the evaluation showed that the device could sample around 1.5 kilo samples per second with greater accuracy if signals are samples at 100Hz or lower. The device yields a good noise performance. The overall cost of the project was around Php 5000.00.

Key Words: Data Acquisition, Industry Standard Architecture Bus, Analog to Digital Converter, Digital to Analog Converter, Computer Interfacing.

LOPE BEN C. PORQUIS Assistant Professor I, Department of Electronics and Communication Engineering, College of Engineering (COE) MSU-IIT. His interests are robotics and hardware development. He hails from Iligan City. OSCAR Y. CHUY, Associate Professor of the Department of Electronics and Communication Engineering, COE, MSU-IIT. His interest is robotics and is from Iligan City.

1. Introduction

The Data Acquisition Card is one of the most important hardware tools in Digital Control and Real Time Signal Processing especially in hardware in-the-loop simulation. The card serves as an interface between the computer and the target prototype. It collects analog signals from the prototype and coverts this signals to digital then streams them into the computer. These digital signals are raw data that represent the responses of the prototype. The computer is processing them and the results are returned to the prototype through the data acquisition card. The concept is just having a communication link between the external device and the computer.

This card-sized data acquisition system was interfaced directly into a computer through the PC's expansion bus (ISA bus). The card is capable of converting analog signal to digital and vice versa. The aim of the design is low cost thus it should be expected that the result would not compete with the existing data acquisition products in the market.

2. Industry Standard Architecture (ISA) BUS

ISA stands for Industry Standard Architecture. In computer science, an unofficial designation for the bus design of the IBM PC/XT, which allows various adaptors to be added to the system by means of inserting plug-in cards into expansion slots. Originally introduced with an 8-bit data path, ISA was expanded in 1984, when IBM introduced the PC/AT, to include a 16-bit data path. Commonly, ISA refers to the expansion slots themselves; such slots are called 8-bit slots or 16-bit slots. A 16-bit slot actually consists of two separate expansion slots mounted end-to-end so that a single 16-bit card plugs into both slots.

An 8-bit expansion card can be inserted and used in a 16-bit slot (it occupies only one of the two slots), but a 16-bit expansion card cannot be used in an 8-bit slot [1].

The advantage of ISA is due to its simplicity. The bus has a separate address and data lines that could make interfacing easier. However the bus runs only at 8MHz and it is no longer available in new computer models today. Even though the bus is history, it still plays an important part in old computer models.

3. Bus Interfacing

The data acquisition card is intended to be plug in directly to the ISA bus. Proper techniques should be done in interfacing the ISA bus. Each device plugged in the ISA bus has its own identity called address. When the computer's processor wants to access a device in the ISA bus it first sends the address of that device. All the devices in the bus will receive that address but the one who can decode it will be the only one who can reply to the processor. The device that responds is called the slave. Usually, the processor is always the master. The slave will send its signals to the CPU through the data lines. There are two basic transactions that can happen between the master and the slave. The READ transaction happens when the master gets the data from the slave. A WRITE transaction does the opposite; the master will send data to the slave.

4. The Data Acquisition Card Design

The figure below shows the block diagram of the data acquisition card.

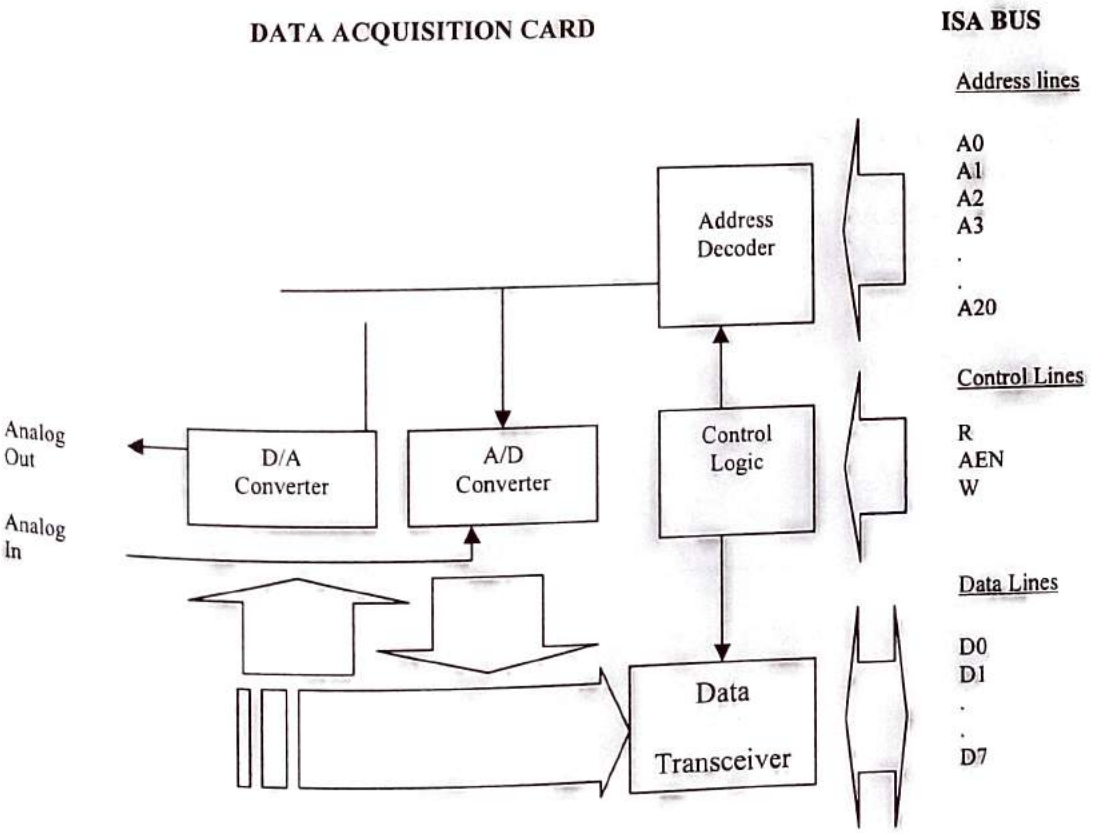

Figure 1. Functional block diagram

The address decoder is a logic circuit that will decode the address 300h (hex). The address 300h is an address space specified by computer designers for prototyping. The decoded signals are used to initiate the two converters. The control logic can determine what type of request the processor sends, whether the request is a READ or a WRITE. During a READ request the decoded signals are intended for the Analog to Digital Converter. In WRITE mode the decoded signals are used to initiate the Digital to Analog Converter. The Data Transceiver will act like a bus switch. It will switch to receive mode at READ request and transmit mode during WRITE request.

5. Evaluation Results

The device was tested by creating a loop back signal channel from the analog to digital converter's (ADC) input to the analog output of the digital to analog converter (DAC). The analog signal enters the ADC's input channel then it is digitized by the converter. The digitized signal will enter the computer through the software driver. The digitized signal can be viewed on the computer monitor screen. The software driver simply returns the digitized data back to the DAC which is converted back to an analog signal. The analog signal coming out from the analog output channel can be observed on the oscilloscope screen. A function generator provides the signal and the oscilloscope was used to view the signal at the analog output. The setup is shown in the following figure.

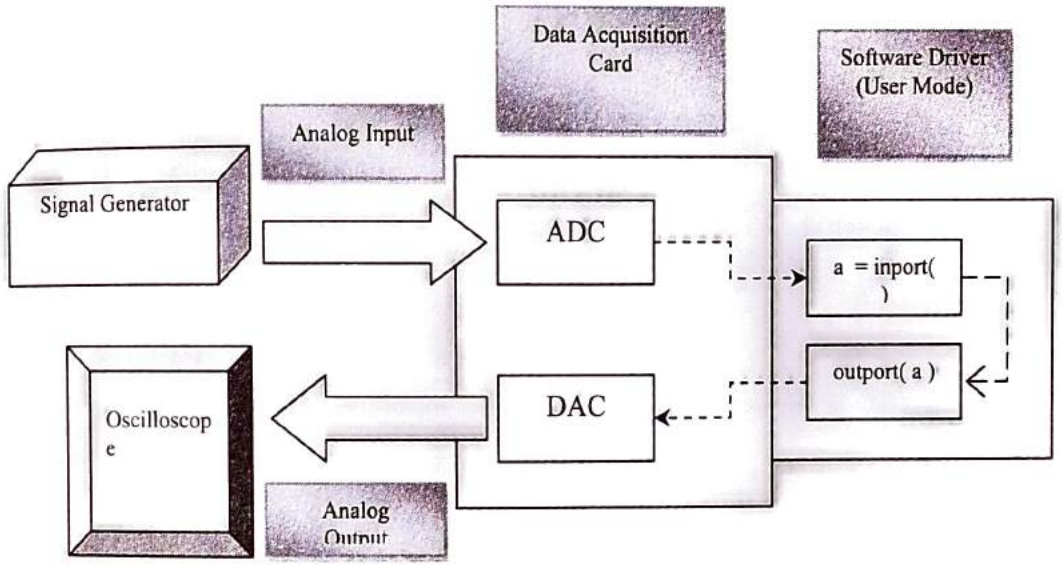

Figure 2. The Evaluation Setup

The following figures show the signal as observed in the oscilloscope screen.

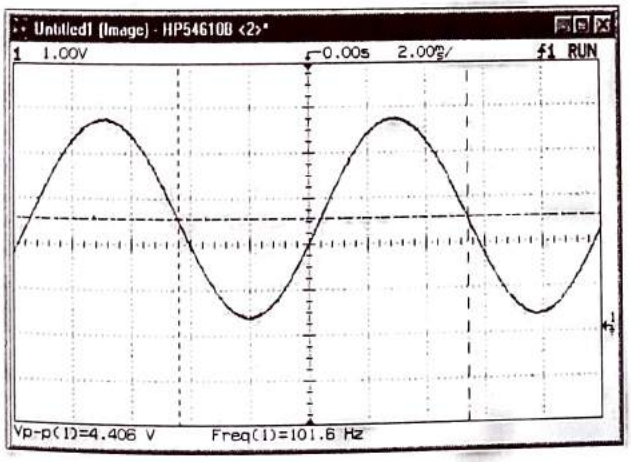

Figure 3. Input signal to the data acquisition card.

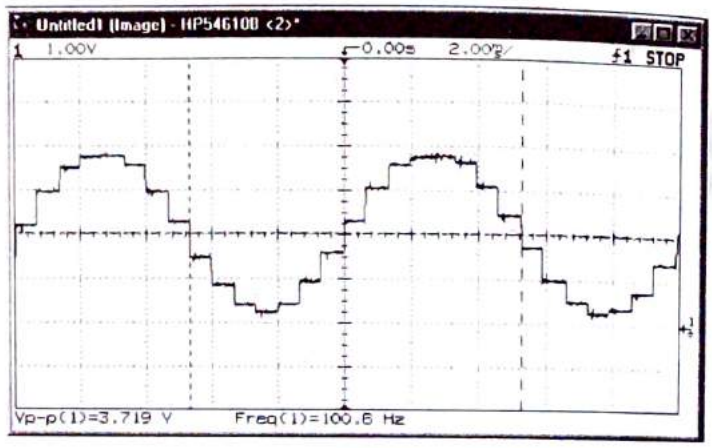

Figure 4. Output signal of the data acquisition card.

In the above figures, the sine wave runs at a frequency of 100Hz. Results showed that the data acquisition card was able to copy the waveform of the signal but it is not very accurate. This inaccuracy resulted from the low sampling rate of the data acquisition card. The sampling rate of the data acquisition card is only 1.5 kilo samples per second. Since the software driver used in this evaluation is developed in user mode, the operation of the data acquisition card is also affected. The speed of execution of a user mode device driver is affected by the number of processes running in the computer. This test was conducted on a PC having a processor frequency of 500MHz, 64MB of RAM and running a Windows 98 operating system.

The succeeding figures show the sampled and reconstructed signal of a sinusoidal and triangular wave running at 60Hz. Channel 1 (output from the data acquisition card) displays the reconstructed signal. Channel 2 (input to the data acquisition card) displays the original signal.

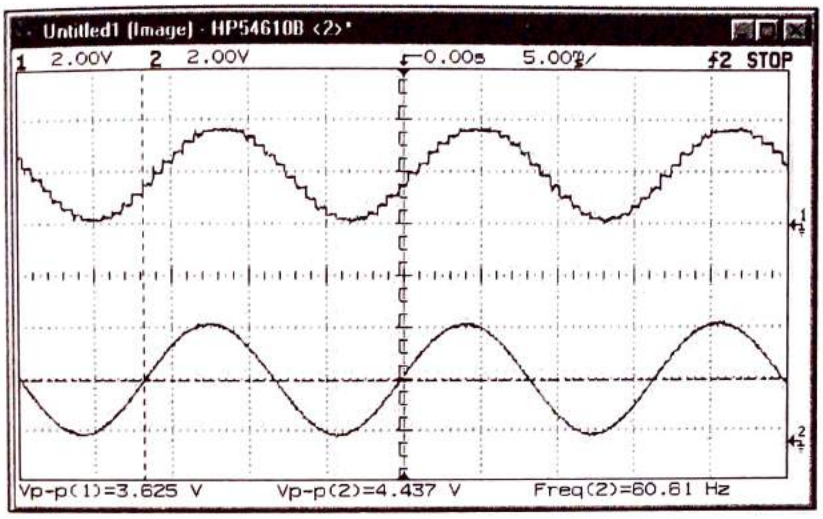

Figure 5. Sine wave at 60Hz

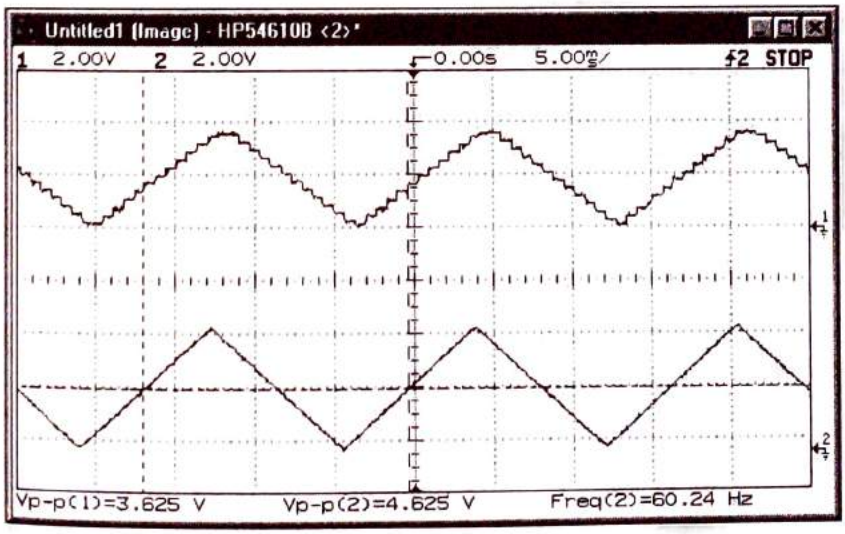

Figure 6. Triangular wave at frequency 60Hz

The reconstructed signal (Channel 1) is more accurate than the previous results. The reason for this is that at 60Hz the rate of change of the slope is slower than that of a 100Hz signal.

In this succeeding figure a sine wave running at a frequency of 25Hz is evaluated.

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